

FIG. 1

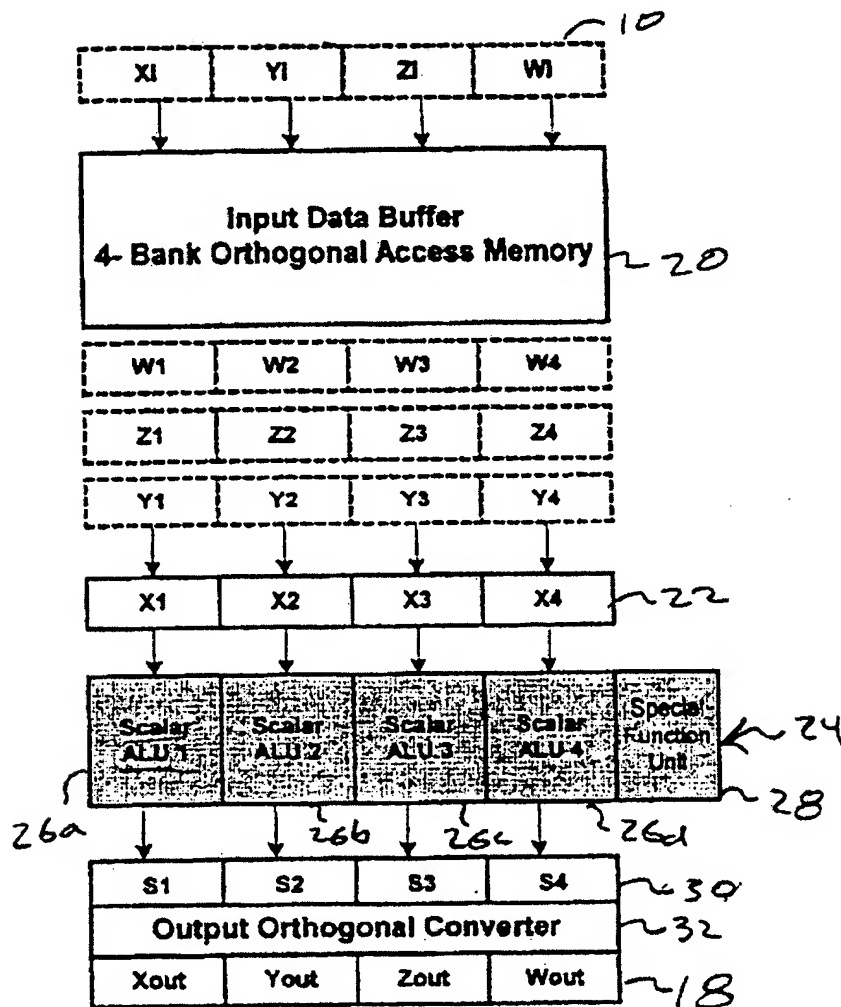


Fig. 2

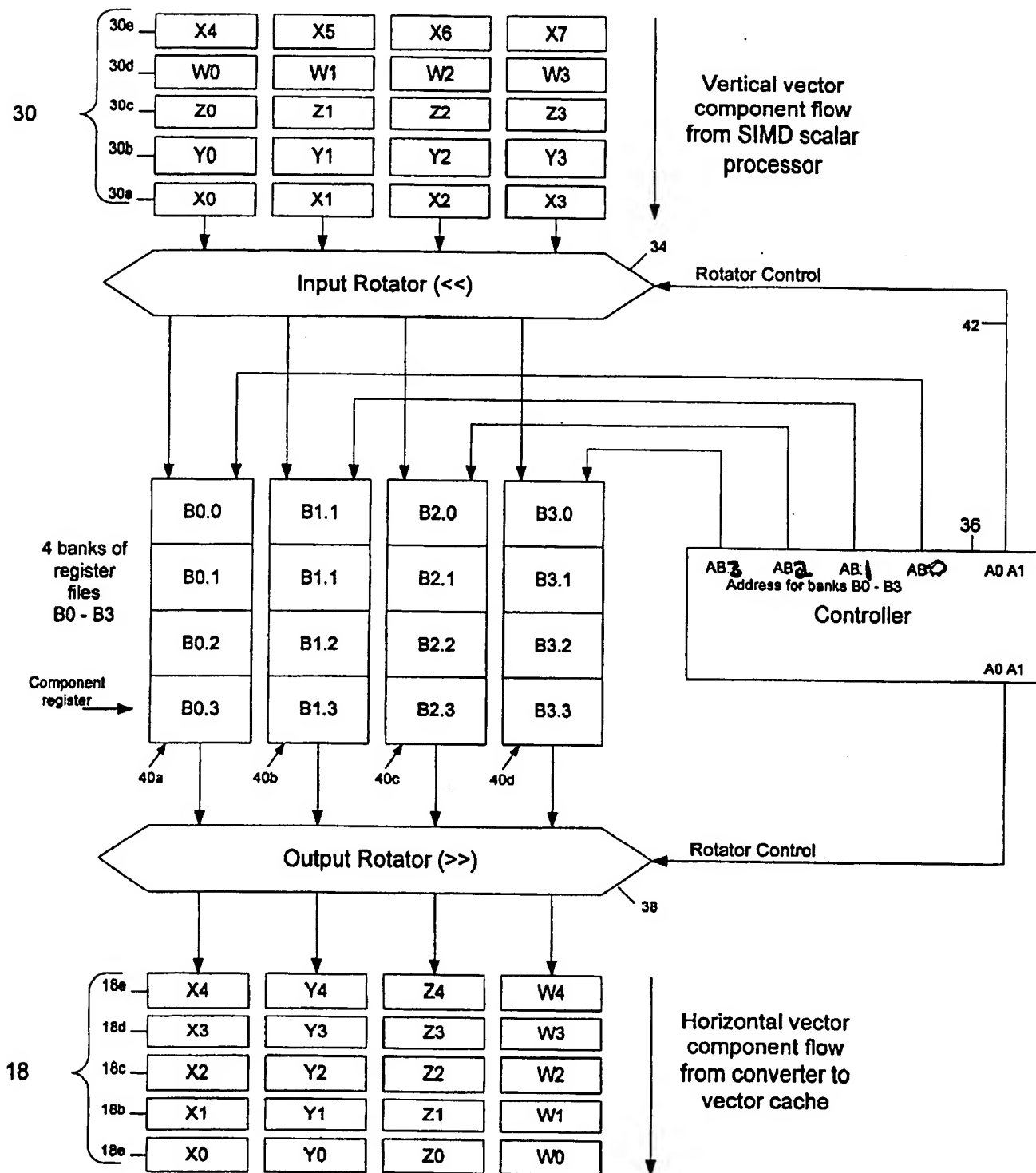


FIG. 3

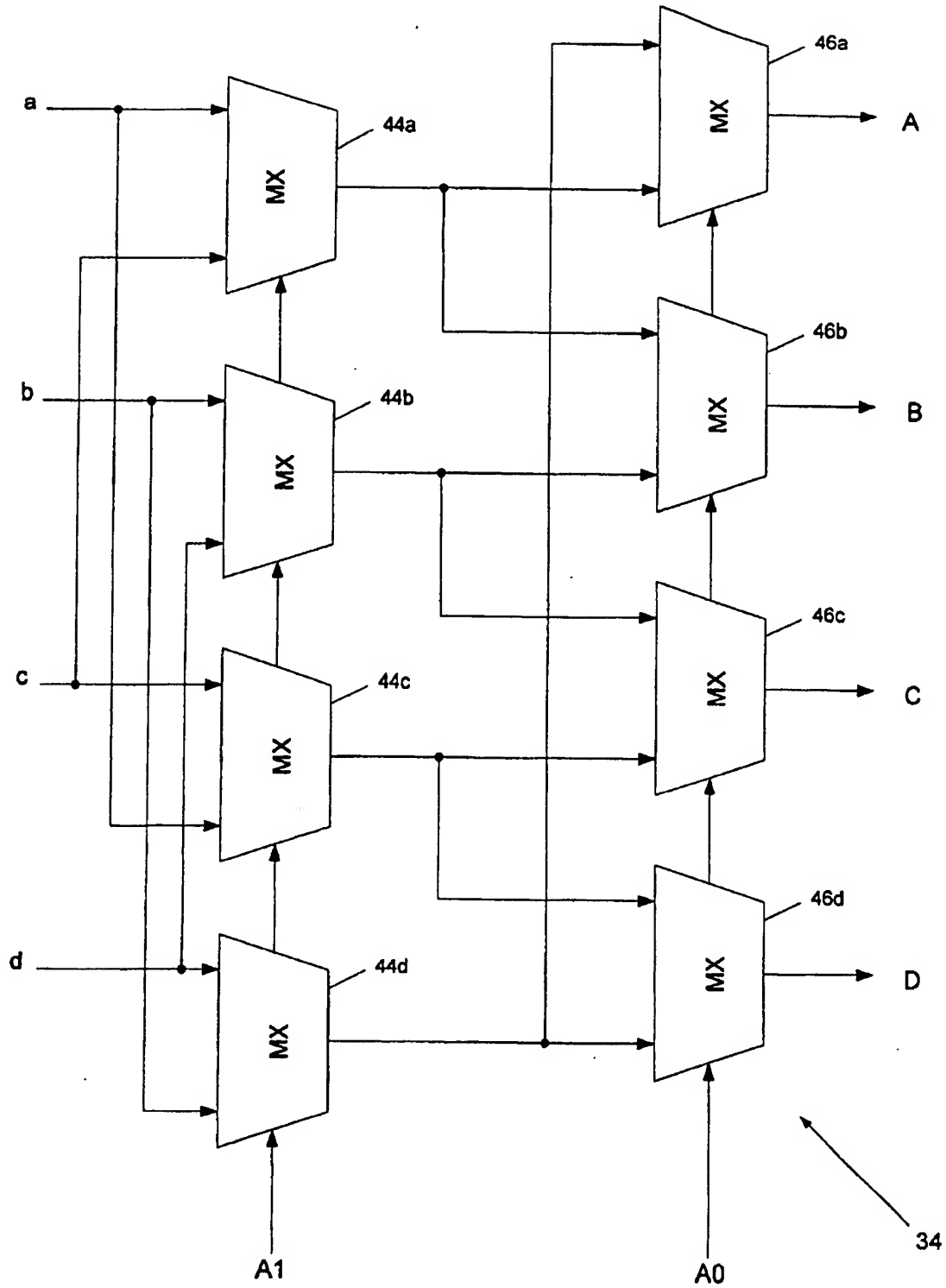


FIG. 4

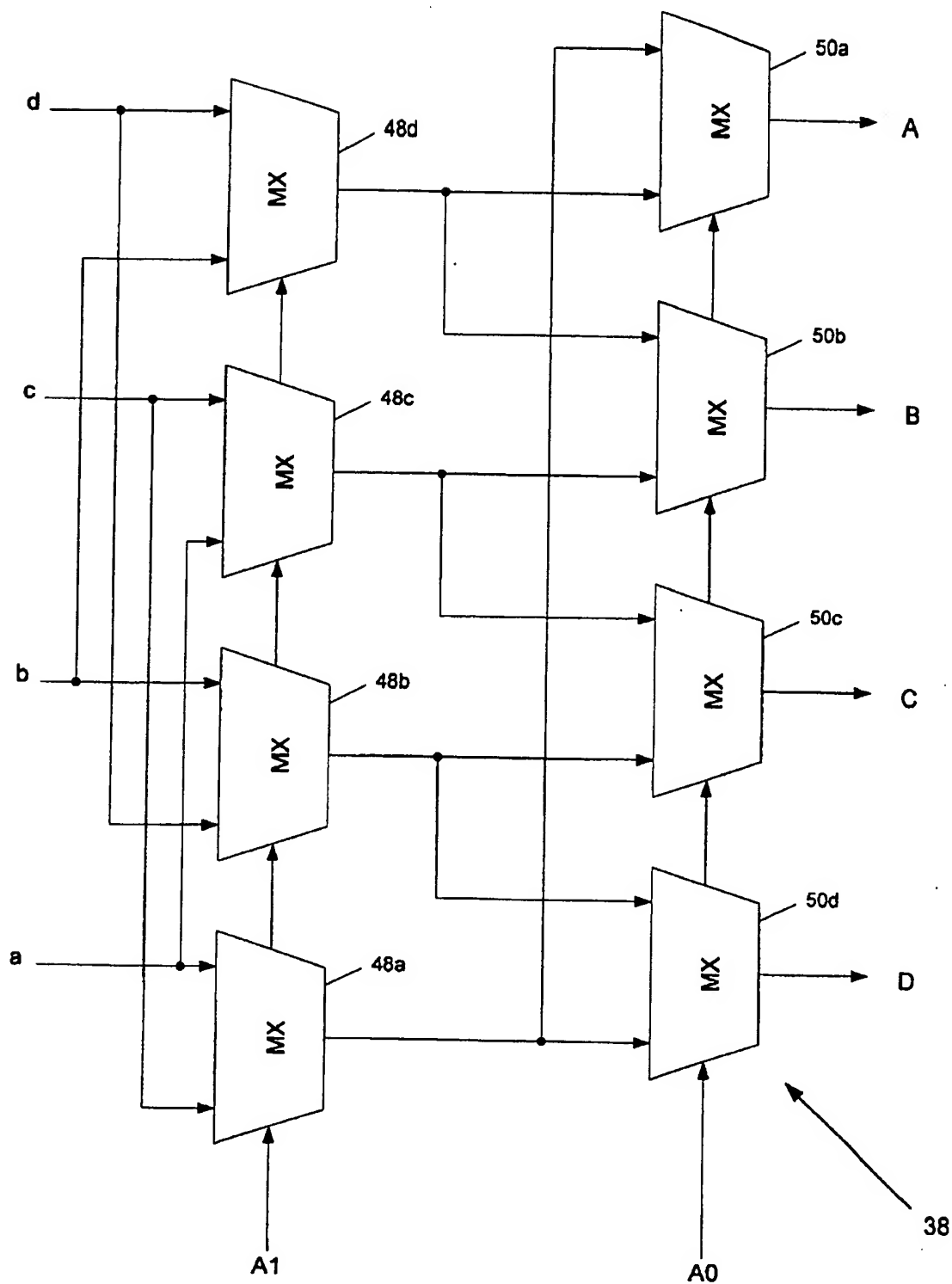


FIG. 5



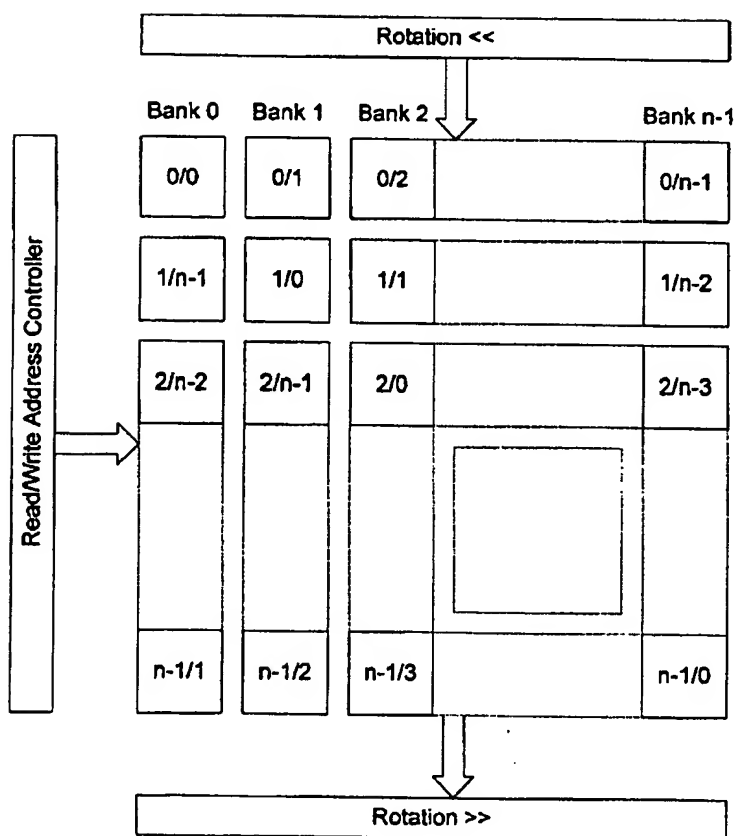


FIG. 7

C	A	B	CAB0	AB0	AB1	AB2	AB3	Input Vector Control	Input Vector Data	Node Input	Output Control	Output Data
1	0	0	0	0	0	0	0	X0 X1 X2 X3	No	Invalid	No	
2	1	1	1	1	1	1	1	Y3 Y0 Y1 Y2	>>1	Invalid		
3	2	2	2	2	2	2	2	Z2 Z3 Z0 Z1	>>2	Invalid		
4	3	3	3	3	3	3	3	W1 W2 W3 W0	>>3	Invalid		
	AB0	AB0	AB0	AB0	AB0	AB0	AB0					
5	0	1	2	3				X4 X5 X6 X7	No	X0 Y0 Z0 W0	No	
6	3	0	1	2				Y7 Y4 Y5 Y6	>>1	W1 X1 Y1 Z1	<<1	
7	2	3	0	1				Z6 Z7 Z4 Z5	>>2	Z2 W2 X2 Y2	<<2	
8	1	2	3	0				W5 W6 W7 W4	>>3	Y3 Z3 W3 X3	<<3	
	AB0	AB0+1	AB0+2	AB0+3								
9	0	0	0	0				X8 X9 X10 X11	No	X4 Y4 Z4 W4	No	
10	1	1	1	1				Y11 Y8 Y9 Y10	>>1	W5 X5 Y5 Z5	<<1	
11	2	2	2	2				Z10 Z11 Z8 Z9	>>2	Z6 W6 X6 Y6	<<2	
12	3	3	3	3				W9 W10 W11 W8	>>3	Y7 W7 Z7 X7	<<3	
	AB0	AB0	AB0	AB0								